US009298720B2

(12) **United States Patent**
Xia et al.

(10) **Patent No.: US 9,298,720 B2**
(45) **Date of Patent: Mar. 29, 2016**

(54) **SYSTEMS AND METHODS FOR FRAGMENTED DATA RECOVERY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 81 days.

(21) Appl. No.: **14/047,441**

(22) Filed: **Oct. 7, 2013**

(65) **Prior Publication Data**

US 2015/0082115 A1 Mar. 19, 2015

Related U.S. Application Data

(60) Provisional application No. 61/878,678, filed on Sep. 17, 2013, provisional application No. 61/885,314, filed on Oct. 1, 2013.

(51) **Int. Cl.**
H03M 13/00 (2006.01)
G06F 17/30 (2006.01)
G06F 11/08 (2006.01)

(52) **U.S. Cl.**
CPC ***G06F 17/30135*** (2013.01); ***G06F 11/085*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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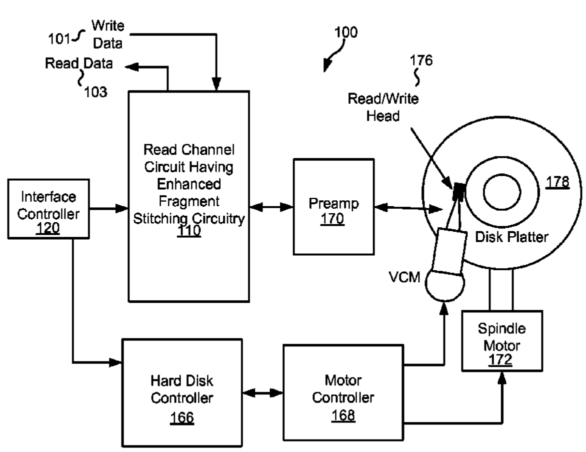
Primary Examiner — Daniel McMahon

(57) **ABSTRACT**

Systems and method relating generally to data processing, and more particularly to systems and methods for fragmenting a data set and recovering the fragmented data set. As one example, a data processing system is discussed that includes: a fragmenting circuit operable to separate a data set into at least a first fragment and a second fragment; and a transfer packet formation circuit operable to: append identification information to the front of the first fragment, and at least a first M+N bits of the second fragment to the end of the first fragment to yield a first transfer fragment, and aggregate the first transfer fragment with other transfer fragments to yield an aggregate output.

17 Claims, 6 Drawing Sheets



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Zhong, "Block-LDPC: A Practical LDPC Coding System Design Approach", IEEE Trans. on Circuits, Regular Papers, vol. 5, No. 4, pp. 766-775, Apr. 2005.

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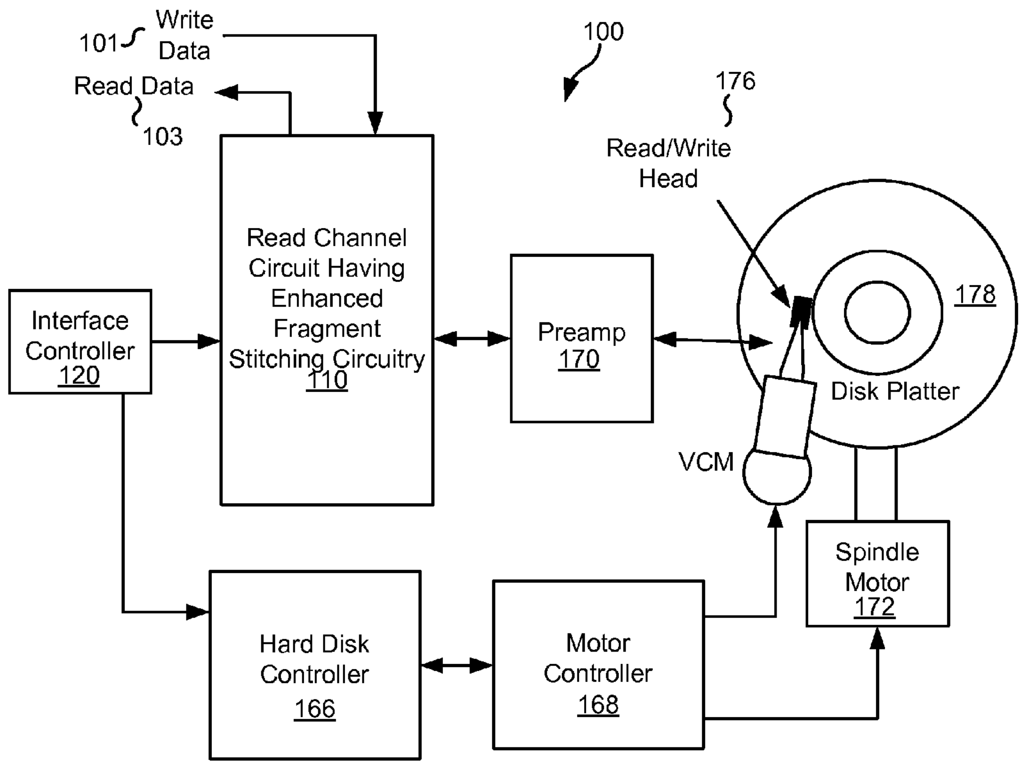
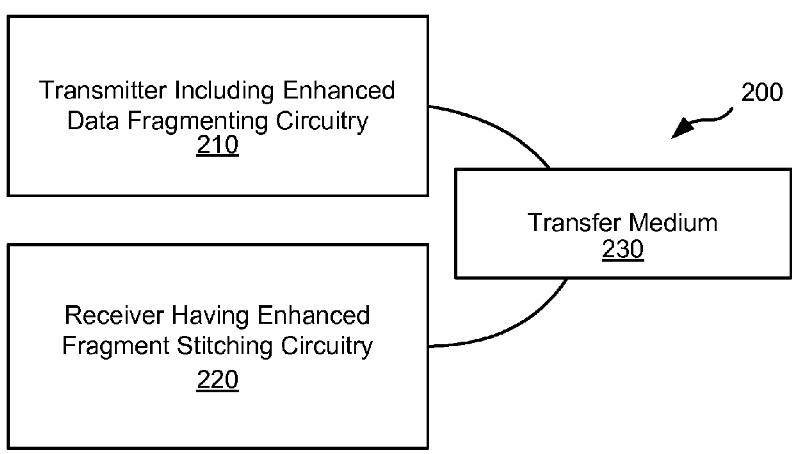


101
Write Data
Read Data
103
100
176
Read/Write Head
Read Channel Circuit Having Enhanced Fragment Stitching Circuitry
110
Interface Controller
120
Preamp
170
178
Disk Platter
VCM
Spindle Motor
172
Hard Disk Controller
166
Motor Controller
168

Fig. 1



Transmitter Including Enhanced Data Fragmenting Circuitry
210
200
Transfer Medium
230
Receiver Having Enhanced Fragment Stitching Circuitry
220

Fig. 2

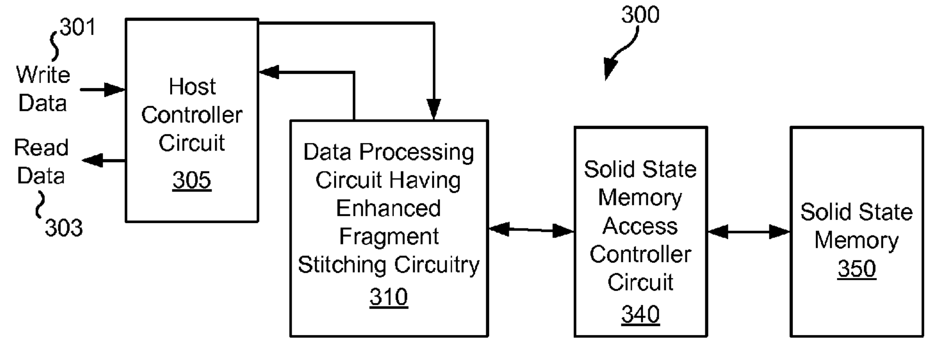

300
301
Write Data
Read Data
303
Host Controller Circuit 305
Data Processing Circuit Having Enhanced Fragment Stitching Circuitry 310
Solid State Memory Access Controller Circuit 340
Solid State Memory 350

Fig. 3

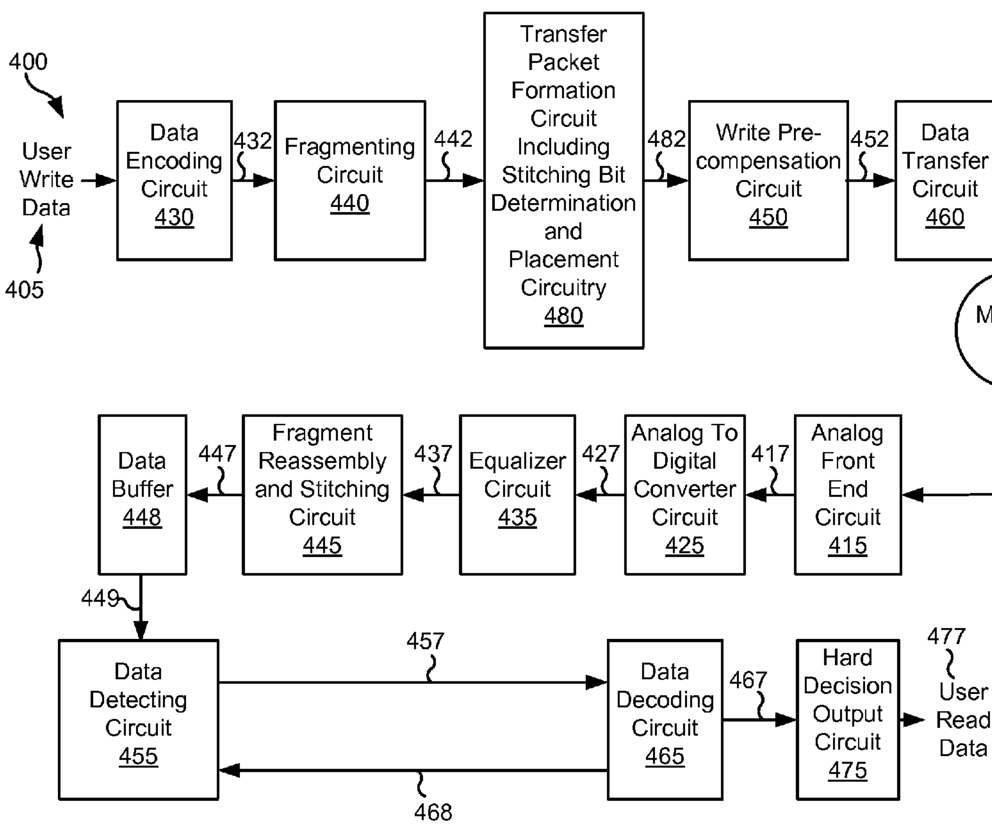

400
User Write Data
405
Data Encoding Circuit 430
432
Fragmenting Circuit 440
442
Transfer Packet Formation Circuit Including Stitching Bit Determination and Placement Circuitry 480
482
Write Pre-compensation Circuit 450
452
Data Transfer Circuit 460
462
Medium 470
472
Analog Front End Circuit 415
417
Analog To Digital Converter Circuit 425
427
Equalizer Circuit 435
437
Fragment Reassembly and Stitching Circuit 445
447
Data Buffer 448
449
Data Detecting Circuit 455
457
468
Data Decoding Circuit 465
467
Hard Decision Output Circuit 475
477
User Read Data

Fig. 4

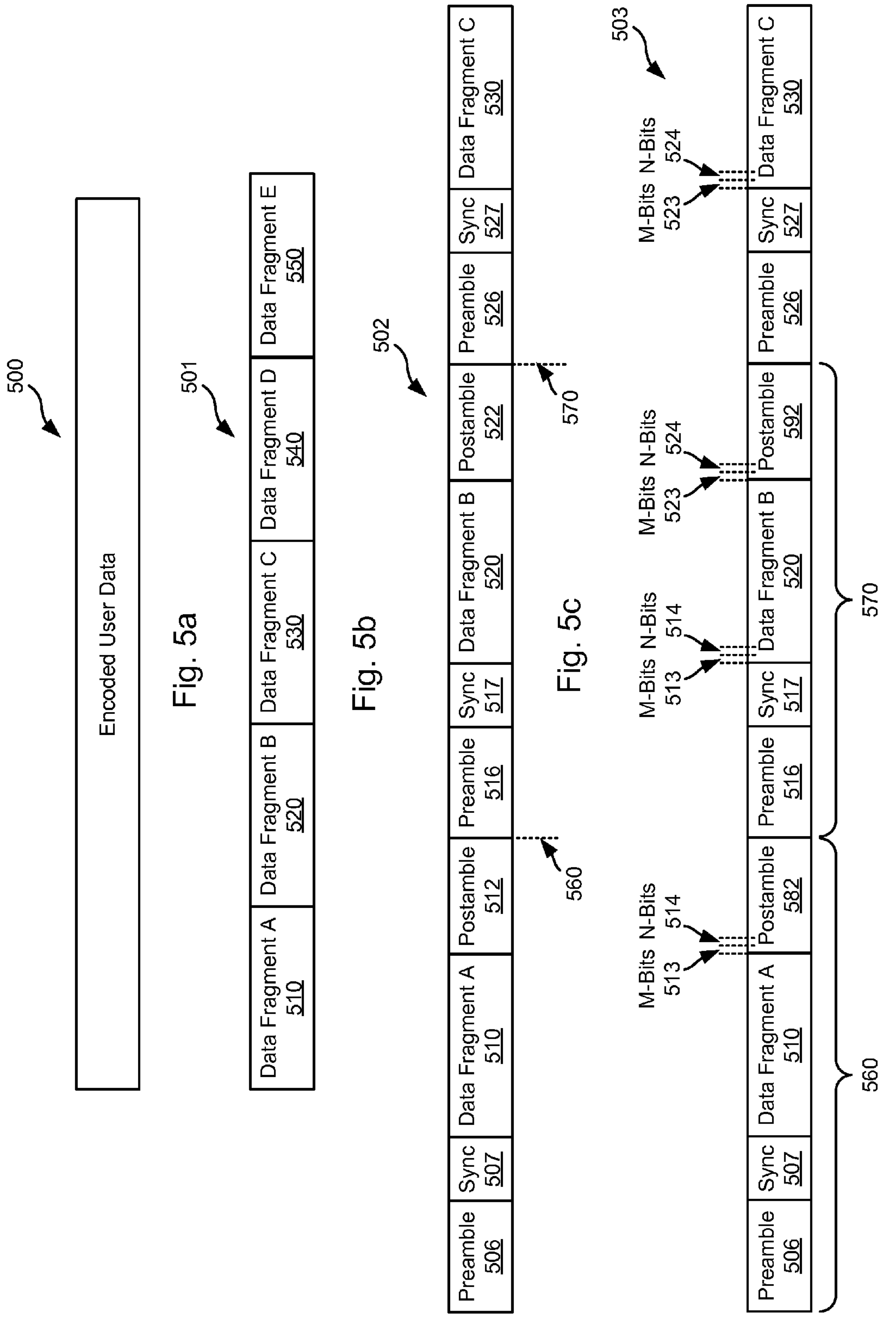


Fig. 5a

Fig. 5b

Fig. 5c

Fig. 5d

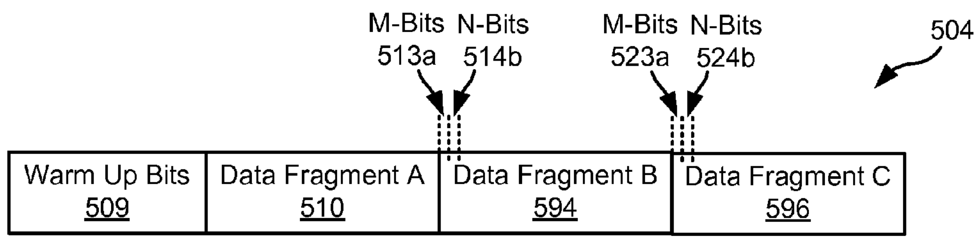

M-Bits
513a
N-Bits
514b
M-Bits
523a
N-Bits
524b
504
Warm Up Bits
509
Data Fragment A
510
Data Fragment B
594
Data Fragment C
596

Fig. 5e

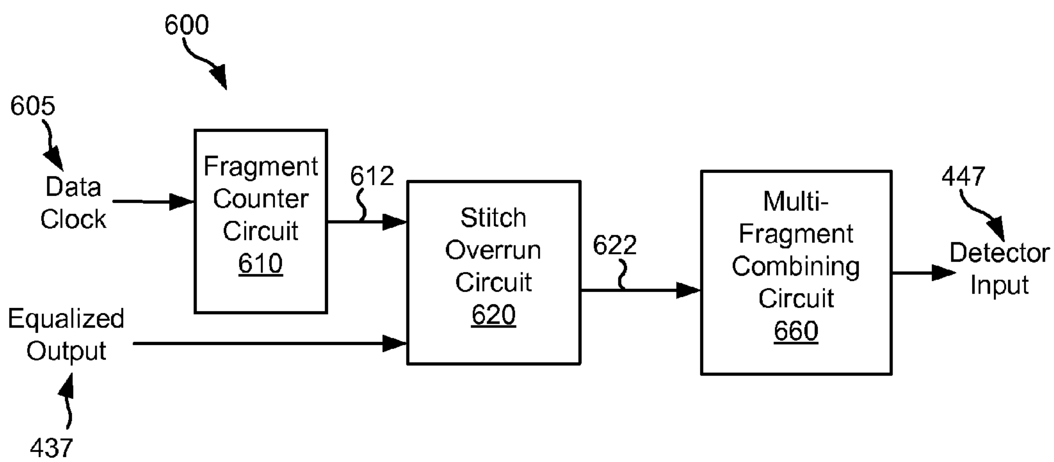

600
605
Data
Clock
Fragment
Counter
Circuit
610
612
Stitch
Overrun
Circuit
620
622
Multi-
Fragment
Combining
Circuit
660
447
Detector
Input
Equalized
Output
437

Fig. 6

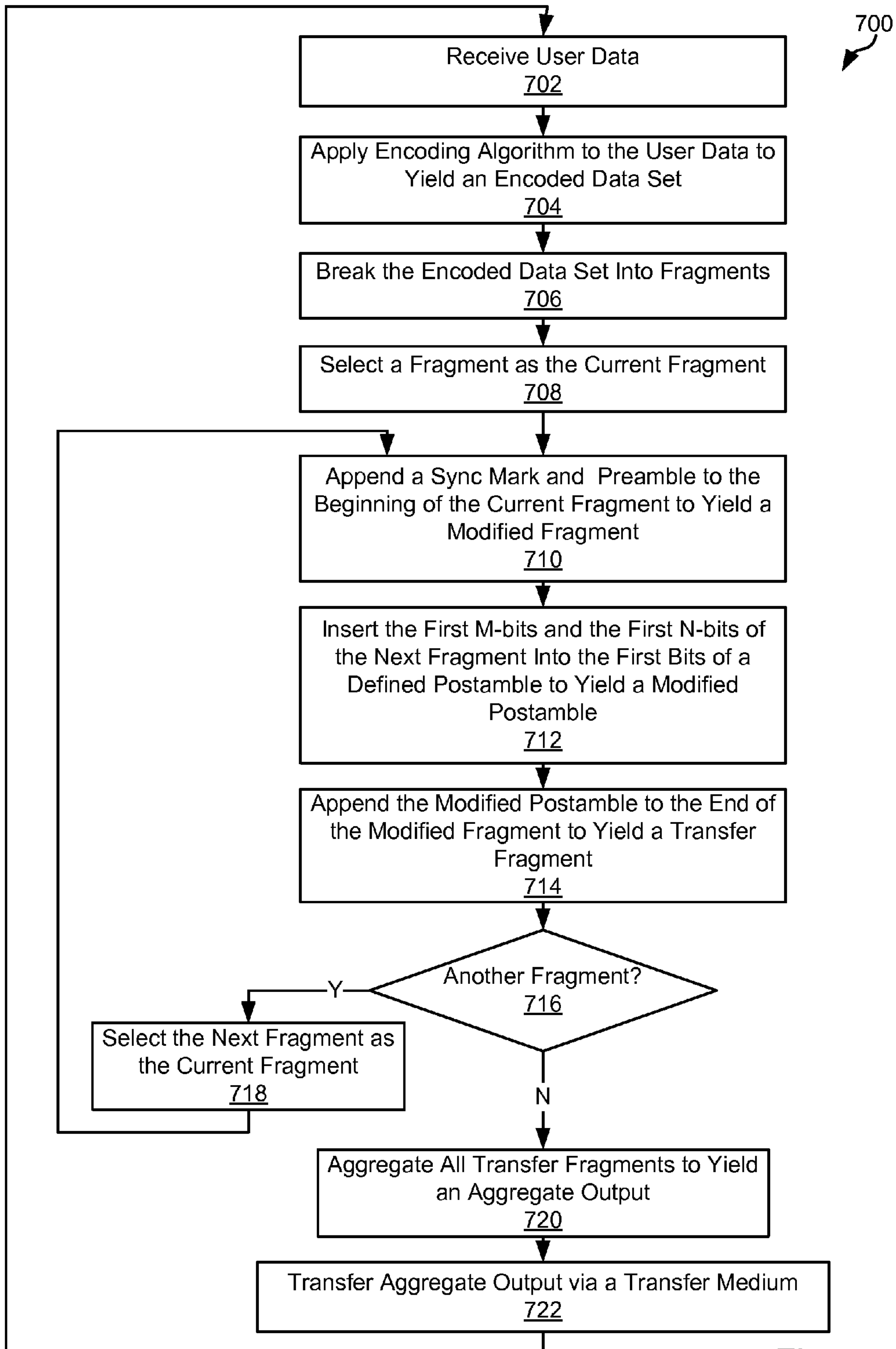

700
Receive User Data
702
Apply Encoding Algorithm to the User Data to Yield an Encoded Data Set
704
Break the Encoded Data Set Into Fragments
706
Select a Fragment as the Current Fragment
708
Append a Sync Mark and Preamble to the Beginning of the Current Fragment to Yield a Modified Fragment
710
Insert the First M-bits and the First N-bits of the Next Fragment Into the First Bits of a Defined Postamble to Yield a Modified Postamble
712
Append the Modified Postamble to the End of the Modified Fragment to Yield a Transfer Fragment
714
Another Fragment?
716
Y
Select the Next Fragment as the Current Fragment
718
N
Aggregate All Transfer Fragments to Yield an Aggregate Output
720
Transfer Aggregate Output via a Transfer Medium
722

Fig. 7

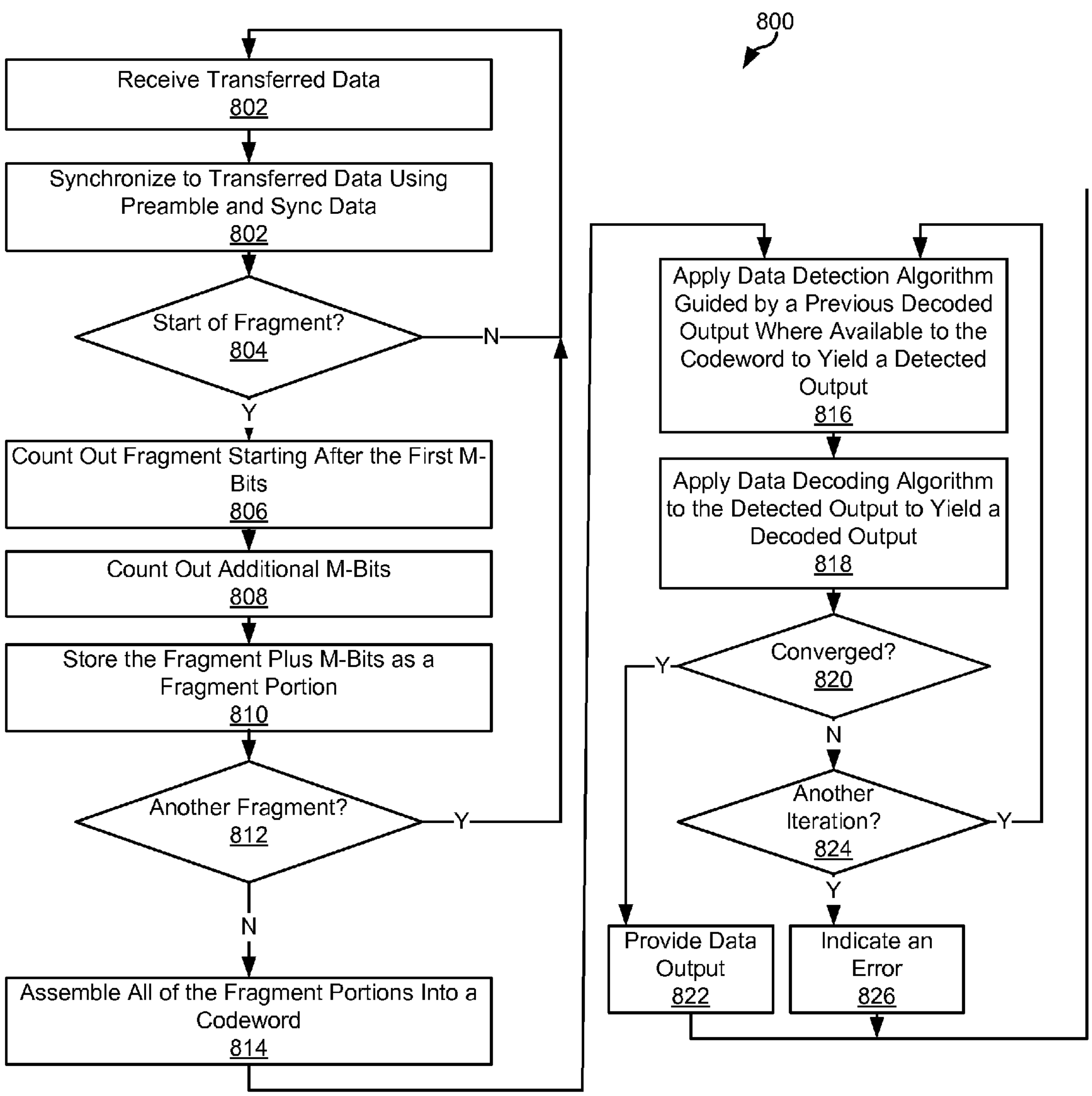

800
Receive Transferred Data
802
Synchronize to Transferred Data Using Preamble and Sync Data
802
Start of Fragment?
804
N
Y
Count Out Fragment Starting After the First M-Bits
806
Count Out Additional M-Bits
808
Store the Fragment Plus M-Bits as a Fragment Portion
810
Another Fragment?
812
Y
N
Assemble All of the Fragment Portions Into a Codeword
814
Apply Data Detection Algorithm Guided by a Previous Decoded Output Where Available to the Codeword to Yield a Detected Output
816
Apply Data Decoding Algorithm to the Detected Output to Yield a Decoded Output
818
Converged?
820
Y
N
Another Iteration?
824
Y
Y
Provide Data Output
822
Indicate an Error
826

Fig. 8

SYSTEMS AND METHODS FOR FRAGMENTED DATA RECOVERY

CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims priority to (is a non-provisional of) U.S. Pat. App. No. 61/878,678 entitled "Systems and Methods for Recovered Data Stitching", and filed Sep. 17, 2013 by Yang et al., and from U.S. Pat. App. No. 61/885,314 entitled "Systems and Methods for Fragmented Data Recovery", and filed Oct. 1, 2013 by Xia et al. The entirety of the aforementioned provisional patent applications is incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

Systems and method relating generally to data processing, and more particularly to systems and methods for fragmenting a data set and recovering the fragmented data set.

BACKGROUND

Data transfer devices often packetize data prior to sending the data across a transfer medium. This transfer medium may be, for example, a data transmission medium or a storage medium. Once the packetized data is received, it is reassembled to yield the original data. In some cases, errors are introduced through the reassembly process.

Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for data processing.

SUMMARY

Systems and method relating generally to data processing, and more particularly to systems and methods for fragmenting a data set and recovering the fragmented data set.

Some embodiments of the present invention provide data processing systems that include: a fragmenting circuit, a transfer packer formation circuit, and a data transfer circuit. The fragmenting circuit is operable to separate a data set into at least a first fragment and a second fragment. The transfer packet formation circuit operable to: append identification information to the front of the first fragment, and at least the first M+N bits of the second fragment to the end of the first fragment to yield a first transfer fragment; and aggregate the first transfer fragment with other transfer fragments to yield an aggregate output. The data transfer circuit operable to transfer the aggregate output via a transfer medium.

This summary provides only a general outline of some embodiments of the invention. The phrases "in one embodiment," "according to one embodiment," "in various embodiments", "in one or more embodiments", "in particular embodiments" and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

A further understanding of the various embodiments of the present invention may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

FIG. **1** shows a storage device including a read channel circuit having enhanced fragment stitching circuitry in accordance with various embodiments of the present invention;

FIG. **2** shows a data transmission device including a receiver having enhanced fragment stitching circuitry in accordance with one or more embodiments of the present invention;

FIG. **3** shows a solid state memory circuit including a data processing circuit having enhanced fragment stitching circuitry in accordance with some embodiments of the present invention;

FIG. **4** shows a data transfer circuit including a fragment reassembly and stitching circuit in accordance with various embodiments of the present invention;

FIGS. **5***a*-**5***e* graphically depict data processing in accordance with some embodiments of the present invention;

FIG. **6** shows a detailed block diagram of a data reassembly and stitching circuit in accordance with one or more embodiments of the present invention;

FIG. **7** is a flow diagram showing a method in accordance with some embodiments of the present invention for fragmenting a data set in preparation for transfer via a transfer medium; and

FIG. **8** is a flow diagram showing a method in accordance with some embodiments of the present invention for re-assembling a previously fragmented data set for backend processing.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

Systems and method relating generally to data processing, and more particularly to systems and methods for fragmenting a data set and recovering the fragmented data set.

Some embodiments of the present invention provide hard disk drives that include: a disk platter, a data write circuit, a head assembly, and a data reading circuit. The data write circuit includes a fragmenting circuit, a transfer packet formation circuit, and a data transfer circuit. The fragmenting circuit is operable to separate a data set into at least a first fragment and a second fragment. The transfer packet formation circuit is operable to: append identification information to the front of the first fragment, and at least the first M+N bits of the second fragment to the end of the first fragment to yield a first transfer fragment; aggregate the first transfer fragment with other transfer fragments to yield an aggregate output. The data transfer circuit is operable to store the aggregate output to the disk platter as a stored information. The head assembly is disposed in relation to the disk platter and operable to sense the stored information on the disk platter, and to provide a signal corresponding to the sensed information. A data reading circuit includes: an analog to digital converter circuit operable to convert the sensed information to a series of digital samples; an equalizer circuit operable to equalize the digital samples to yield an equalized output, wherein the equalized output includes a first fragment of data and a second fragment of data; a stitching circuit, and a data recovery circuit. The stitching circuit is operable to: receive the stored information including at least a first fragment and a second fragment, where the first M-bits of the second fragment are received both as the first M-bits after the end of the first fragment and as the first M-bits of the second fragment; generating a modified second fragment based on the second fragment from the data set, wherein the first M-bits of the second fragment are derived from the first M-bits after the end of the first fragment; and aggregate the modified second fragment with other modified fragments to yield a codeword. The data recovery circuit is operable to process the codeword to yield an original data set. In some instances of the aforementioned embodiments, the data recovery circuit includes: a data detector circuit operable to apply a data detection algorithm to the codeword to yield a detected output; and a data decoder circuit operable to apply a data decoding algorithm to a decoder input to yield a decoded output, wherein the decoder input is derived from the detected output.

Other embodiments of the present invention provide data processing systems that include: a fragmenting circuit, a transfer packer formation circuit, and a data transfer circuit. The fragmenting circuit is operable to separate a data set into at least a first fragment and a second fragment. The transfer packet formation circuit operable to: append identification information to the front of the first fragment, and at least the first M+N bits of the second fragment to the end of the first fragment to yield a first transfer fragment; and aggregate the first transfer fragment with other transfer fragments to yield an aggregate output. The data transfer circuit operable to transfer the aggregate output via a transfer medium.

In some instances of the aforementioned embodiments, at least one of the value of M and the value of N is programmable. In various instances of the aforementioned embodiments, the identification information includes a preamble pattern and synchronization data. In one or more instances of the aforementioned embodiments, the data processing system is implemented as part of a storage device, and the medium is a storage medium. In other instances of the aforementioned embodiments, the data processing system is implemented as part of a communication device, and the medium is a communication medium. In particular cases, the communication medium is a wireless communication medium. In yet other instances of the aforementioned embodiments, the data processing system is implemented as part of an integrated circuit. Yet other instances of the aforementioned embodiments include a data encoding circuit operable to apply a data encoding algorithm to an input to yield the data set. In some cases, the data encoding algorithm is a low density parity check algorithm.

Yet other embodiments of the present invention provide data processing systems that include: a stitching circuit, and a data recovery circuit. The stitching circuit operable to: receive a data set including at least a first fragment and a second fragment, where the first M-bits of the second fragment are received both as the first M-bits after the end of the first fragment and as the first M-bits of the second fragment; generate a modified second fragment based on the second fragment from the data set, where the first M-bits of the second fragment are derived from the first M-bits after the end of the first fragment; and aggregate the modified second fragment with other modified fragments to yield a codeword. The data recovery circuit is operable to process the codeword to yield an original data set.

In some instances of the aforementioned embodiments, the data set includes a postamble including the first M-bits of the second fragment at the end of the first fragment, and the data set includes identification information between the postamble and the second fragment. In some cases, the identification information includes a preamble pattern and synchronization data. In various instances of the aforementioned embodiments, the value of M is programmable. In one or more instances of the aforementioned embodiments, the data processing system may be implemented as, but is not limited to, a storage device, or a communication device. In some instances of the aforementioned embodiments, the data processing system is implemented as part of an integrated circuit. In various instances of the aforementioned embodiments, the data recovery circuit includes: a data detector circuit operable to apply a data detection algorithm to the codeword to yield a detected output; and a data decoder circuit operable to apply a data decoding algorithm to a decoder input to yield a decoded output, where the decoder input is derived from the detected output.

Turning to FIG. **1**, a storage system **100** is shown that includes a read channel **110** having enhanced fragment stitching circuitry in accordance with one or more embodiments of the present invention. Storage system **100** may be, for example, a hard disk drive. Storage system **100** also includes a preamplifier **170**, an interface controller **120**, a hard disk controller **166**, a motor controller **168**, a spindle motor **172**, a disk platter **178**, and a read/write head **176**. Interface controller **120** controls addressing and timing of data to/from disk platter **178**, and interacts with a host controller (not shown). The data on disk platter **178** consists of groups of magnetic signals that may be detected by read/write head assembly **176** when the assembly is properly positioned over disk platter **178**. In one embodiment, disk platter **178** includes magnetic signals recorded in accordance with either a longitudinal or a perpendicular recording scheme.

In a typical read operation, read/write head **176** is accurately positioned by motor controller **168** over a desired data track on disk platter **178**. Motor controller **168** both positions read/write head **176** in relation to disk platter **178** and drives spindle motor **172** by moving read/write head assembly **176** to the proper data track on disk platter **178** under the direction of hard disk controller **166**. Spindle motor **172** spins disk platter **178** at a determined spin rate (RPMs). Once read/write head **176** is positioned adjacent the proper data track, magnetic signals representing data on disk platter **178** are sensed by read/write head **176** as disk platter **178** is rotated by spindle motor **172**. The sensed magnetic signals are provided as a continuous, minute analog signal representative of the magnetic data on disk platter **178**. This minute analog signal is transferred from read/write head **176** to read channel circuit **110** via preamplifier **170**. Preamplifier **170** is operable to amplify the minute analog signals accessed from disk platter **178**. In turn, read channel circuit **110** decodes and digitizes the received analog signal to recreate the information originally written to disk platter **178**. This data is provided as read data **103** to a receiving circuit. A write operation is substantially the opposite of the preceding read operation with write data **101** being provided to read channel circuit **110**. This data is then encoded and written to disk platter **178**.

In operation, data written to disk platter **178** is split into fragments or portions, and the fragments are augmented with synchronization information to yield a modified fragment. In addition, data from the beginning of the next fragment is appended to the end of the modified fragment as part of a postamble. Multiple modified fragments covering all of the fragments into which the data was originally split are concatenated and transferred via to disk platter **178**. The transferred data is then read back from disk platter **178**, disaggregated, and the individual fragments re-assembled to yield a defragmented data set. This defragmenting includes adding data from the postamble to individual fragments in a stitching operation that reduces the effects of discontinuity between fragments on the backend processing. The fragmenting and de-fragmenting may be done using a circuit similar to that discussed below in relation to FIG. **4** and/or FIG. **6**, and/or the processing may be performed similar to the methods described below in relation to FIG. **7** and FIG. **8**.

It should be noted that storage system **100** may be integrated into a larger storage system such as, for example, a RAID (redundant array of inexpensive disks or redundant array of independent disks) based storage system. Such a RAID storage system increases stability and reliability through redundancy, combining multiple disks as a logical unit. Data may be spread across a number of disks included in the RAID storage system according to a variety of algorithms and accessed by an operating system as if it were a single disk. For example, data may be mirrored to multiple disks in the RAID storage system, or may be sliced and distributed across multiple disks in a number of techniques. If a small number of disks in the RAID storage system fail or become unavailable, error correction techniques may be used to recreate the missing data based on the remaining portions of the data from the other disks in the RAID storage system. The disks in the RAID storage system may be, but are not limited to, individual storage systems such as storage system **100**, and may be located in close proximity to each other or distributed more widely for increased security. In a write operation, write data is provided to a controller, which stores the write data across the disks, for example by mirroring or by striping the write data. In a read operation, the controller retrieves the data from the disks. The controller then yields the resulting read data as if the RAID storage system were a single disk.

A data decoder circuit used in relation to read channel circuit **110** may be, but is not limited to, a low density parity check (LDPC) decoder circuit as are known in the art. Such low density parity check technology is applicable to transmission of information over virtually any channel or storage of information on virtually any media. Transmission applications include, but are not limited to, optical fiber, radio frequency channels, wired or wireless local area networks, digital subscriber line technologies, wireless cellular, Ethernet over any medium such as copper or optical fiber, cable channels such as cable television, and Earth-satellite communications. Storage applications include, but are not limited to, hard disk drives, compact disks, digital video disks, magnetic tapes and memory devices such as DRAM, NAND flash, NOR flash, other non-volatile memories and solid state drives.

In addition, it should be noted that storage system **100** may be modified to include solid state memory that is used to store data in addition to the storage offered by disk platter **178**. This solid state memory may be used in parallel to disk platter **178** to provide additional storage. In such a case, the solid state memory receives and provides information directly to read channel circuit **110**. Alternatively, the solid state memory may be used as a cache where it offers faster access time than that offered by disk platted **178**. In such a case, the solid state memory may be disposed between interface controller **120** and read channel circuit **110** where it operates as a pass through to disk platter **178** when requested data is not available in the solid state memory or when the solid state memory does not have sufficient storage to hold a newly written data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of storage systems including both disk platter **178** and a solid state memory.

Turning to FIG. **2**, a data transmission system **200** including a receiver **220** enhanced fragment stitching circuitry in accordance with one or more embodiments of the present invention. Transmitter **210** including enhanced data fragmenting circuitry that splits data into fragments or portions, and the fragments are augmented with synchronization information to yield a modified fragment. Transmitter **210** transmits the modified fragments via a transfer medium **230** as is known in the art. The encoded data is received from transfer medium **230** by receiver **220**.

During operation, data sent via transfer medium **230** is split into fragments or portions by transmitter **210**, and the fragments are augmented with synchronization information to yield a modified fragment. In addition, data from the beginning of the next fragment is appended to the end of the modified fragment as part of a postamble. Multiple modified fragments covering all of the fragments into which the data was originally split are concatenated and transferred via transfer medium **230**. The transferred data is received by receiver **220** and disaggregated and the individual fragments re-assembled to yield a de-fragmented data set. This defragmenting includes adding data from the postamble to individual fragments in a stitching operation that reduces the effects of discontinuity between fragments on the backend processing. The fragmenting and de-fragmenting may be done using a circuit similar to that discussed below in relation to FIG. **4** and/or FIG. **6**, and/or the processing may be performed similar to the methods described below in relation to FIG. **7** and FIG. **8**.

Turning to FIG. **3**, another storage system **300** is shown that includes a data processing circuit **310** having enhanced slice stitching circuitry in accordance with one or more embodiments of the present invention. A host controller circuit **305** receives data to be stored (i.e., write data **301**). This data is segregated into fragments or portions by data processing circuit **310** prior to being transferred to a solid state memory access controller circuit **340**. The fragments are augmented with synchronization information to yield a modified fragment. In addition, data from the beginning of the next fragment is appended to the end of the modified fragment as part of a postamble. Multiple modified fragments covering all of the fragments into which the data was originally split are concatenated and transferred to the solid state memory access controller circuit **340**. The transferred data may then be read from the solid state memory access controller **340**, disaggregated, and the individual fragments re-assembled to yield a de-fragmented data set. This defragmenting includes adding data from the postamble to individual fragments in a stitching operation that reduces the effects of discontinuity between fragments on the backend processing. The fragmenting and de-fragmenting may be done using a circuit similar to that discussed below in relation to FIG. **4** and/or FIG. **6**, and/or the processing may be performed similar to the methods described below in relation to FIG. **7** and FIG. **8**.

Turning to FIG. **4**, a data transfer circuit **400** is shown that includes a fragment reassembly and stitching circuit **445** in accordance with one or more embodiments of the present invention. Data transfer circuit **400** includes a data encoding circuit **430** that is operable to apply a data encoding algorithm to user write data **405** to yield an encoded output **432**. In some embodiments of the present invention, data encoding circuit **430** applies a low density parity check encoding algorithm as is known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of encoding algorithms and/or combinations of encoding algorithms that may be implemented in accordance with different embodiments of the present invention.

Turning to FIG. **5***a*, an encoded user data set **500** is shown as an example of encoded output **432**. Retuning to FIG. **4**, encoded output **432** is provided to a fragmenting circuit **440** that segregates encoded output **432** into a number of fragments or portions that are provided as a portion output **442** to a transfer packet formation circuit **480**. Transfer packet formation circuit **480** includes stitching bit determination and placement circuitry. Turning to FIG. **5***b*, a fragmented data set **501** is shown that includes a data fragment A **510**, a data fragment B **520**, data fragment C **530**, data fragment D **540**, and data fragment E **550**. Fragmented data set **501** is an example of portion output **442** of FIG. **4**.

Referring again to FIG. **4**, transfer packet formation circuit **480** operates to append a preamble and synchronization data to the beginning of each data fragment in portion output **442**, and to append a postamble to the end of each data fragment in portion **442**. The preamble may be a periodic pattern useful for frequency and phase adjustment of a sampling circuit as is known in the art. In one particular embodiment of the present invention, the periodic pattern is a "2T pattern" (i.e., '110011001100 . . . '). The synchronization data may be a defined sync code used to indicate the beginning of an associated fragment. Turning to FIG. **5***c*, a modified fragment set **502** including: fragment A **510** modified to be preceded by a preamble **506** and synchronization data **507**, and to be followed by a postamble **512**; fragment B **520** modified to be preceded by a preamble **516** and synchronization data **517**, and to be followed by a postamble **522**; and fragment C **530** modified to be preceded by a preamble **526** and synchronization data **527**, and to be followed by a postamble (not shown). Referring again to FIG. **4**, transfer packet formation circuit **480** additionally takes M+N bits of data from the beginning of the next data fragment and uses them to replace the first M+N bits of the postamble following the current data fragment to yield a modified postamble. In some embodiments of the present invention, the value of M is programmable, while in other embodiments the value is fixed. Similarly, in some embodiments of the present invention, the value of N is programmable, while in other embodiments the value is fixed. In one particular embodiment of the present invention the value is M is three (3) and the value of N is three (3). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of values that may be used for M and N in accordance with different embodiments of the present invention. The combination of adding preamble, synchronization and modified postamble data to a data fragment results in a transfer fragment. This process is repeated for a number of data fragments corresponding to encoded output **432**. Each of the resulting transferred fragments are concatenated one to another to yield an aggregate output **482**. Turning to FIG. **5***d*, an aggregate output **503** is depicted that includes a number of transfer fragments (**560**, **570**) that each include a preamble, synchronization data, a data fragment, and a modified postamble. In particular, transfer fragment **560** includes preamble **506**, synchronization data **507**, data fragment A **510**, and a modified postamble **582**; and transfer fragment **570** includes preamble **516**, synchronization data **517**, data fragment B **520**, and a modified postamble **592**. Modified postamble **582** includes the first M bits **513** from data fragment B **520** and the first N bits **514** from data fragment B **520** replacing the first M+N bits of postamble **512**. Similarly, modified postamble **592** includes the first M bits **523** from data fragment C **530** and the first N bits **524** from data fragment C **530** replacing the first M+N bits of postamble **522**. Aggregate output **503** is an example of a portion of aggregate output **482**.

Referring again to FIG. **4**, aggregate output **482** is provided to a write pre-compensation circuit **450**. Write pre-compensation circuit **450** generates a compensated output **452** that is provided to a data transfer circuit **460**. Data transfer circuit **460** may be any circuit capable of providing the received information to a transfer medium **470** as a data output **462**. As such, data transfer circuit **460** may be, but is not limited to, a solid state storage device write circuit, a magnetic storage device write circuit, or a data transmission circuit.

Data output **462** is received by an analog front end circuit **415** from medium **470** as a read input **472**. Analog front end circuit **415** processes read input **472** to yield a processed analog signal **417** that is provided to an analog to digital converter circuit **425**. Analog front end circuit **415** may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit **415**. Analog to digital converter circuit **425** converts processed analog signal **417** into a corresponding series of digital samples **427**. Analog to digital converter circuit **425** may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples **427** are provided to an equalizer circuit **435**. Equalizer circuit **435** applies an equalization algorithm to digital samples **427** to yield an equalized output **437**. In some embodiments of the present invention, equalizer circuit **435** is a digital finite impulse response filter circuit as are known in the art.

Equalized output **437** is provided to fragment reassembly and stitching circuit **445**. Fragment reassembly and stitching circuit **445** is operable to separate the data fragments from the preamble, synchronization and postamble data. Then replaces the first M-bits of each data fragment with the first M-bits of the preceding postamble. As the first M+N bits of the preceding postamble are the first M+N bits of the data fragment prior to transfer, this results in substantially the same M+N bits at the beginning of each data fragment, and provides a continuous transition between the last bits of the preceding data fragment and the first M-bits of the current data fragment, and a reasonably continuous transition between the first M-bits of the current data fragment and the next N-bits of the current data fragment. In addition, fragment reassembly and stitching circuit **445** adds warm up bits prior to the first data fragment to allow for adjustment to the transition to the first part of the data fragment. In some cases, these warm up bits are the first bit of the first fragment replicated a number of times. The result is a stitched codeword similar to encoded output **432** plus any noise introduced during processing and transfer via medium **470**. Turning to FIG. **5***e*, a stitched codeword **504** is shown that includes warm up bits **509**, data fragment A **510**, a modified data fragment B **594**, and a modified data fragment C **596**. Modified data fragment B **594** includes the first M-bits **513***a* of modified postamble **582** as they exist after processing and transfer replacing the first M-bits of data fragment B **520** followed by the next N-bits **514***b* of data fragment B **520** as they exist after processing and transfer. Similarly, modified data fragment C **596** includes the first M-bits **523***a* of modified postamble **592** as they exist after processing and transfer replacing the first M-bits of data fragment C **530** followed by the next N-bits **524***b* of data fragment C **530** as they exist after processing and transfer. Stitched codeword **504** is an example of a portion of stitched codeword **447**.

FIG. **6**, is a block diagram of a data reassembly and stitching circuit **600** in accordance with one or more embodiments of the present invention. Data reassembly and stitching circuit **600** may be used in place of fragment reassembly and stitching circuit **445**. Data reassembly and stitching circuit **600** includes a fragment counter circuit **610** that is incremented as each instance of equalized output **437** is received. The resulting count value **612** indicates the beginning and end of fragments in equalized output **437**. Once the end of a fragment is indicated by count value **612**, fragment counter circuit **610** is reset to indicate the beginning of the next fragment.

Count value **612** is provided to a stitch overrun circuit **620** that includes M-bits from the postamble of the preceding fragment to be maintained as the first M-bits of the next data fragment indicated by count value **612**. A resulting stitched codeword **622** (including the first M-bits of the preceding postamble replacing the first M-bits of the next data fragment) is provided to a multi-fragment combining circuit **660**. Multi-fragment combining circuit **660** combines multiple fragments together to yield stitched codeword **447**.

Stitched codeword **447** is stored to a data buffer **448** where it awaits backend processing through a data detecting circuit **455** and a data decoding circuit **465**. In particular, a detector input **449** from data buffer **448** is provided to data detecting circuit **455**. Data detecting circuit **455** may be any circuit known in the art that is capable of apply a data detection algorithm to a data set to yield a detected output. As some examples, data detecting circuit **455** may be, but is not limited to, a Viterbi algorithm detector circuit or a maximum a posteriori detector circuit as are known in the art. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detecting circuits that may be used in relation to different embodiments of the present invention. Detected output **457** may include both hard decisions and soft decisions. The terms "hard decisions" and "soft decisions" are used in their broadest sense. In particular, "hard decisions" are outputs indicating an expected original input value (e.g., a binary '1' or '0', or a non-binary digital value), and the "soft decisions" indicate a likelihood that corresponding hard decisions are correct. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of hard decisions and soft decisions that may be used in relation to different embodiments of the present invention.

Detected output **457** is provided to data decoding circuit **465** that applies a data decoding algorithm to the received input to yield a decoded output **467**. In one particular embodiment of the present invention, data decoding circuit **465** is operable to apply a low density parity check decoded circuit. Where decoded output **467** fails to converge (i.e., fails to reflect the original data), it is provided as a feedback **468** to data detecting circuit **455** to apply another iteration of the combination of data detecting circuit **455** and data decoding circuit **465**. Alternatively, where decoded output **467** does converge (i.e., reflects the original data), it is provided to a hard decision output circuit **475** that provides the resulting hard decisions as user read data **477**.

Turning to FIG. **7**, a flow diagram **700** shows a method in accordance with some embodiments of the present invention for fragmenting a data set in preparation for transfer via a transfer medium. Following flow diagram **700**, a user data set is received (block **702**). An encoding algorithm is applied to the received user data to yield an encoded data set (block **704**). In one particular embodiment of the present invention, the encoding algorithm is a low density parity check encoding algorithm as is known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize other encoding algorithms that may be used in relation to different embodiments of the present invention. The encoded data set is broken into fragments (block **706**). The size of the fragments may be predefined. FIG. **5***b* shows a fragmented data set **501** as an example of the result of block **706**. As shown, fragmented data set **501** includes a data fragment A **510**, a data fragment B **520**, data fragment C **530**, data fragment D **540**, and data fragment E **550**.

A first fragment from the fragmented data set is selected as a current fragment (block **708**). A synchronization mark and a preamble are appended to the beginning of the current fragment to yield a modified fragment (block **710**). In addition, the first M+N bits of the next fragment are used to replace the first M+N bits of a defined postamble to yield a modified postamble (block **712**). The modified postamble is then appended to the end of the modified fragment to yield a transfer fragment (block **714**). FIG. **5***d* shows an example of such a transfer fragment as transfer fragment **560** that includes preamble **506**, synchronization data **507**, data fragment A **510**, and a modified postamble **582**.

It is then determined whether another fragment remains to be converted to a transfer fragment (block **716**). Where another fragment remains to be converted (block **716**), the next fragment is selected as the current fragment (block **718**). Then, the processes of blocks **710-718** are repeated for the next fragment. Alternatively, where no additional fragments remain to be converted (block **716**), all of the recently prepared transfer fragments are aggregated to yield an aggregate output (block **720**). FIG. **5***d* shows an example of such an aggregate output as aggregate output **503** that includes a number of transfer fragments (**560**, **570**) that each include a preamble, synchronization data, a data fragment, and a modified postamble. In particular, transfer fragment **560** includes preamble **506**, synchronization data **507**, data fragment A **510**, and modified postamble **582**; and transfer fragment **570** includes preamble **516**, synchronization data **517**, data fragment B **520**, and modified postamble **592**. Modified postamble **582** includes the first M bits **513** from data fragment B **520** and the first N bits **514** from data fragment B **520** replacing the first M+N bits of postamble **512**. Similarly, modified postamble **592** includes the first M bits **523** from data fragment C **530** and the first N bits **524** from data fragment C **530** replacing the first M+N bits of postamble **522**. Aggregate output **503** is an example of a portion of aggregate output **482**. The value of one or both of M and N may be programmable or fixed. In one particular embodiment of the present invention the value is M is three (3) and the value of N is three (3). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of values that may be used for M and N in accordance with different embodiments of the present invention.

The aggregated output may be transferred via a medium (block **722**). The medium may be, but is not limited to, a storage medium, a wireless communication medium, or a wired communication medium. Such a storage medium may be, but is not limited to, an optical storage medium, a magnetic storage medium, or a solid state storage medium. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize different mediums that may be used in relation to different embodiments of the present invention.

Turning to FIG. **8**, a flow diagram **800** shows a method in accordance with some embodiments of the present invention for re-assembling a previously fragmented data set for back-end processing. Following flow diagram **800**, transferred data is received (block **802**). FIG. **5***d* shows an example of such transferred data as aggregate output **503** that includes a number of transfer fragments (**560**, **570**) that each include a preamble, synchronization data, a data fragment, and a modified postamble. In particular, transfer fragment **560** includes preamble **506**, synchronization data **507**, data fragment A **510**, and modified postamble **582**; and transfer fragment **570** includes preamble **516**, synchronization data **517**, data fragment B **520**, and modified postamble **592**. Modified postamble **582** includes the first M bits **513** from data fragment B **520** and the first N bits **514** from data fragment B **520** replacing the first M+N bits of postamble **512**. Similarly, modified postamble **592** includes the first M bits **523** from data fragment C **530** and the first N bits **524** from data fragment C **530** replacing the first M+N bits of postamble **522**. Aggregate output **503** is an example of a portion of aggregate output **482**. The value of one or both of M and N may be programmable or fixed. In one particular embodiment of the present invention the value is M is three (3) and the value of N is three (3). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of values that may be used for M and N in accordance with different embodiments of the present invention.

The preamble and synchronization data is used to synchronize to the received data (block **802**). Based upon the finding of a preamble followed by the synchronization data the beginning of a fragment can be determined. It is determined whether the start of a fragment is indicated (block **804**). Where the start of a fragment is indicated (block **804**), the instances of the fragment are counted after the first M-bits (block **806**) plus an additional M-bits (block **808**), and the fragment plus M-bits is stored as a fragment portion (block **810**). Doing such results in the first M-bits of the postamble being included as the first M-bits of the next fragment.

It is determined whether another fragment remains to be processed (block **812**). Where another fragment remains to be processed (block **812**), the processes beginning at block **802** are performed to process the next segment. Alternatively, where no additional fragments remain to be processed (block **812**), all of the fragment portions are assembled into a codeword (block **814**). An example of a portion of such a codeword is shown in FIG. **5***e* as stitched codeword **504**. As shown, stitched codeword **504** includes warm up bits **509**, data fragment A **510**, a modified data fragment B **594**, and a modified data fragment C **596**. Modified data fragment B **594** includes the first M-bits **513***a* of modified postamble **582** as they exist after processing and transfer replacing the first M-bits of data fragment B **520** followed by the next N-bits **514***b* of data fragment B **520** as they exist after processing and transfer. Similarly, modified data fragment C **596** includes the first M-bits **523***a* of modified postamble **592** as they exist after processing and transfer replacing the first M-bits of data fragment C **530** followed by the next N-bits **524***b* of data fragment C **530** as they exist after processing and transfer.

A data detection algorithm is applied to the codeword to yield a detected output (block **816**). Where available, application of the data detection algorithm is guided by a previous decoded output. The data detection algorithm may be any data detection algorithm known in the art including, but not limited to, a Viterbi data detection algorithm or a maximum a posteriori data detection algorithm. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detection algorithms that may be used in relation to different embodiments of the present invention.

A data decoding algorithm is applied to the detected output to yield a decoded output (block **818**). The data decoding algorithm may be, for example, a low density parity check decoding algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data decoding algorithms that may be used in relation to different embodiments of the present invention. It is determined whether application of the data decoding algorithm converged (block **820**). Where the algorithm converged (no errors remain) (block **820**), the decoded output is provided as a data output (block **822**). Otherwise, where the algorithm failed to converge (errors remain) (block **820**), it is determined whether another iteration applying the data detection algorithm and the data decoding algorithm is desired (block **824**). Where another iteration is desired (block **824**), the processes of blocks **816**-**822** are repeated. Alternatively, where no additional iterations are desired (block **824**), an error is indicated (block **826**).

It should be noted that the various blocks discussed in the above application may be implemented in integrated circuits along with other functionality. Such integrated circuits may include all of the functions of a given block, system or circuit, or a subset of the block, system or circuit. Further, elements of the blocks, systems or circuits may be implemented across multiple integrated circuits. Such integrated circuits may be any type of integrated circuit known in the art including, but are not limited to, a monolithic integrated circuit, a flip chip integrated circuit, a multichip module integrated circuit, and/or a mixed signal integrated circuit. It should also be noted that various functions of the blocks, systems or circuits discussed herein may be implemented in either software or firmware. In some such cases, the entire system, block or circuit may be implemented using its software or firmware equivalent. In other cases, the one part of a given system, block or circuit may be implemented in software or firmware, while other parts are implemented in hardware.

In conclusion, the invention provides novel systems, devices, methods and arrangements for data processing. While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A hard disk drive, the hard disk drive comprising:
- a disk platter;
- a data write circuit including:
  - a fragmenting circuit operable to separate a data set into at least a first fragment and a second fragment;
  - a transfer packet formation circuit operable to:
    - append identification information to the front of the first fragment, and at least a first M+N bits of the second fragment to the end of the first fragment to yield a first transfer fragment; and
    - aggregate the first transfer fragment with other transfer fragments to yield an aggregate output; and
  - a data transfer circuit operable to store the aggregate output to the disk platter as a stored information;
- a head assembly disposed in relation to the disk platter and operable to:
  - sense the stored information on the disk platter to yield a sensed information;

provide a signal corresponding to the sensed information;

a data reading circuit including:

an analog to digital converter circuit operable to convert the sensed information to a series of digital samples;

an equalizer circuit operable to equalize the series of digital samples to yield an equalized output, wherein the equalized output includes the first fragment of data and the second fragment of data;

a stitching circuit operable to:

receive the stored information including at least a first fragment and a second fragment, wherein the first M-bits of the second fragment are received both as the first M-bits after the end of the first fragment and as the first M-bits of the second fragment;

generate a modified second fragment based on the second fragment from the stored information, wherein a first M-bits of the second fragment are derived from a first M-bits after the end of the first fragment;

aggregate the modified second fragment with other modified fragments to yield a codeword; and

a data recovery circuit operable to process the codeword to yield an original data set.

2. The hard disk drive of claim **1**, wherein the data recovery circuit comprises:

a data detector circuit operable to apply a data detection algorithm to the codeword to yield a detected output; and

a data decoder circuit operable to apply a data decoding algorithm to a decoder input to yield a decoded output, wherein the decoder input is derived from the detected output.

3. The hard disk drive of claim **1**, wherein at least one of the value of M and the value of N is programmable.

4. The hard disk drive of claim **1**, wherein the identification information includes a preamble pattern and synchronization data.

5. The hard disk drive of claim **1**, wherein the system further comprises: a data encoding circuit operable to apply a data encoding algorithm to an input to yield the data set.

6. The hard disk drive of claim **5**, wherein the data encoding algorithm is a low density parity check algorithm.

7. A data storage device, the system comprising:

a disk platter;

a data reading circuit including:

an analog to digital converter circuit operable to convert sensed information derived from the disk platter to a series of digital samples;

an equalizer circuit operable to equalize the series of digital samples to yield an equalized output, wherein the equalized output includes a data set including at least a first fragment and second fragment;

a stitching circuit operable to:

receive the data set, wherein a first M-bits of the second fragment are received both as the first M-bits after the end of the first fragment and as the first M-bits of the second fragment;

generate a modified second fragment based on the second fragment from the data set, wherein the first M-bits of the second fragment are derived from the first M-bits after the end of the first fragment;

aggregate the modified second fragment with other modified fragments to yield a codeword; and

a data recovery circuit operable to process the codeword to yield an original data set.

8. The data storage device of claim **7**, wherein the data set includes a postamble including the first M-bits of the second fragment at the end of the first fragment, and wherein the data set includes identification information between the postamble and the second fragment.

9. The data storage device of claim **8**, wherein the identification information includes a preamble pattern and synchronization data.

10. The data storage device of claim **7**, wherein the value of M is programmable.

11. The data storage device processing system of claim **7**, wherein the data recovery circuit comprises:

a data detector circuit operable to apply a data detection algorithm to the codeword to yield a detected output; and

a data decoder circuit operable to apply a data decoding algorithm to a decoder input to yield a decoded output, wherein the decoder input is derived from the detected output.

12. The data storage device of claim **11**, wherein the data detection algorithm is selected from a group consisting of: a maximum a posteriori data detection algorithm, and a Viterbi data detection algorithm.

13. The data storage device of claim **11**, wherein the data decoding algorithm is a low density parity check algorithm.

14. A storage device, the system comprising:

a disk platter;

a data write circuit including:

a fragmenting circuit operable to separate a data set into at least a first fragment and a second fragment;

a transfer packet formation circuit operable to:

append identification information to the front of the first fragment, and at least a first M+N bits of the second fragment to the end of the first fragment to yield a first transfer fragment; and

aggregate the first transfer fragment with other transfer fragments to yield an aggregate output; and

a data transfer circuit operable to store the aggregate output to the disk platter as a stored information.

15. The storage device of claim **14**, wherein at least one of the value of M and the value of N is programmable.

16. The storage device of claim **14**, wherein the system further comprises:

a data encoding circuit operable to apply a data encoding algorithm to an input to yield the data set.

17. The storage device of claim **14**, wherein the data encoding algorithm is a low density parity check algorithm.

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